REMARKS

Summary of the Office Action

Claims 1-6 and 23-28 were pending in the above-identified patent application. Claims 7-22 were withdrawn from consideration pursuant to applicants' reply to the restriction requirement of December 15, 2005. Applicants cancelled withdrawn claims 7-22, without prejudice.

Claims 1 and 23 are objected to for containing various informalities.

Claims 1-6 and 23-28 are provisionally rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 20-26 of co-pending Application No. 09/924,272 (hereinafter "the '272 application").

Claims 1-6 and 23-28 are rejected under 35 U.S.C. § 102(b) as being anticipated by Agarwal et al. U.S. Patent No. 5,761,484.

Summary of Applicants' Reply

Applicants have amended claims 1-6 and 23-28 and added new claims 29 and 30 to more particularly define the invention. No new matter has been added and the amendments and new claims are fully supported by the originally filed specification. For example, support for these amendments and new claims may be found on page 2, line 28 through page 3, line 20 and page 37, line 34 through page 38, line 9 of applicants' specification.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Applicants' Reply to the Claim Objections

Claims 1 and 23 are objected to for containing various informalities. In particular, the Examiner objected to the phrases "possible optimizations," "a more efficient

implementation, "a program," "software constructs," and "where using software constructs comprises establishing communications between the programmable logic circuit and at least one software device," as being uncertain and unclear.

Applicants respectfully submit that amended independent claims 1 and 23 do not contain these alleged informalities. Accordingly, applicants respectfully request that the objection to claims 1 and 23 be withdrawn.

Applicants' Reply to the Provisional Obviousness-Type Double Patenting Rejection

Claims 1-6 and 23-28 are provisionally rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 20-26 of co-pending Application No. 09/924,272. The Examiner should continue to make this "provisional" double patenting rejection as long as there are conflicting claims in these two applications unless the "provisional" double patenting rejection is the only rejection remaining in this application. If the "provisional" double patenting rejection is the only rejection remaining in this application, then the Examiner should withdraw the rejection and permit this application to issue as a patent, thereby converting the "provisional" double patenting rejection in the other application into a double patenting rejection at the time when this application issues as a patent. See MPEP § 804(I)(B).

Applicants' Reply to the Rejections under 35 U.S.C. § 102(b)

Claims 1-6 and 23-28 are rejected under 35 U.S.C. § 102(b) as being anticipated by Agarwal.

Amended independent claims 1 and 23 are directed toward a method and a software-to-hardware compiler for generating an optimized circuit that implements a program implemented in programmable logic. A programmable logic

circuit that implements a program is generated and analyzed for optimizations. This analysis includes determining whether to split the program into a hardware portion implemented in the programmable logic circuit and a software portion implemented in at least one software processor. The programmable logic circuit is then optimized to provide a more efficient implementation of the program by modifying the programmable logic circuit to execute the software portion of the program on the at least one software processor. Finally, communications are established between the optimized programmable logic circuit and the at least one software processor.

Agarwal refers to a reconfigurable logic system having virtual interconnections in order to overcome device pin limitations. In other words, each physical wire may be multiplexed amongst multiple logical wires thereby increasing the usable bandwidth of the logic device.

However, Agarwal does not show "determining whether to split the program into a hardware portion implemented in the programmable logic circuit and a software portion implemented in at least one software processor" and optimizing the programmable logic circuit by "modifying the programmable logic circuit to execute the software portion of the program using the at least one software processor," as specified by applicants' amended independent claims 1 and 23.

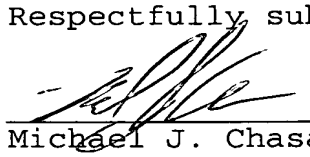
Accordingly, for at least this reason, applicants respectfully request that the rejection of independent claims 1 and 23 be withdrawn.

Applicants also submit that claims 2-6 and 24-30 variously depend from independent claims 1 and 23 and are allowable at least because claims 1 and 23 are allowable.

Conclusion

The foregoing demonstrates that this application is in condition for allowance. Accordingly, reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,



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